

CLAIMS

What is claimed is:

Sub
C4
fig. 7
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1. A circuit device comprising:
a first transistor including a first metal gate electrode
overlying [a over] a first gate dielectric on a first area of a
semiconductor substrate and having a work function corresponding
to the work function of one of P-type silicon and N-type
silicon; and

a second transistor complementary to the first transistor
including a second metal gate electrode over a second gate
dielectric on a second area of a semiconductor substrate and
having a work function corresponding to the work function of the
other one of P-type silicon and N-type silicon.

2. The integrated circuit device of claim 1, wherein the first
metal gate electrode is one of a pure metal, a doped metal, and
a metal alloy.

3. A method of forming a circuit device, comprising:
forming a gate dielectric overlying a region of a
substrate;
depositing a metal layer over the gate dielectric; and
modifying the Fermi level of the metal layer.

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1 4. The method of claim 3, further comprising the step of
2 patterning the metal layer into a gate electrode.

1 5. The method of claim 3, wherein the step of modifying the
2 Fermi level of the metal layer includes chemically reacting the
3 metal layer with a compound.

1 6. The method of claim 5, wherein the region of the substrate
2 includes a first region and a second region, and prior to the
3 step of modifying the first metal layer, the method further
4 comprises the step of:
5 masking the metal layer over the second region.

1 7. The method of claim 6, wherein the masking step includes
2 masking with an inert compound.

1 8. The method of claim 6, wherein the masking step includes
2 masking with a masking compound that reacts with the metal layer
3 over the second region to modify the Fermi level of the reaction
4 product.

1 9. The method of claim 8, wherein the masking compound is
2 polysilicon.

1 10. The method of claim 3, wherein the step of modifying the
2 Fermi level of the metal layer includes alloying the metal layer
3 with one of a second metal layer and a silicon.

1 11. The method of claim 10, wherein the region of the substrate
2 includes a first region and a second region, and the step of
3 modifying the metal layer comprises modifying one of the first
4 region and the second region.

1 12. The method of claim 11, wherein the step of alloying the
2 metal layer includes alloying with a polysilicon.

1 13. The method of claim 3, wherein the step of modifying the
2 Fermi level of the metal layer includes implanting an ion into
3 the metal layer.

1 14. The method of claim 13, wherein the region of the substrate
2 includes a first region and a second region, and the step of
3 modifying the metal layer comprises modifying one of the first
4 region and the second region.

1 15. The method of claim 14, wherein after the step of modifying
2 the metal layer of one of the first region and the second
3 region, the method comprises the step of modifying the other of
4 the first region and the second region.

add(5)
add 1a